Intel Technology Briefing

November 7, 2000

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What are we talking about?

An important milestone

- Successful completion of 0.13㎛m (130 nanometer) generation logic technology development
- Intel has built functional SRAMs and microprocessors using 130nm design rules -- first to demonstrate operating integrated circuits on this technology
- New process will allow Intel to build processors with >100 million transistors and will operate at multi-GHz

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Logic Process Evolution

	P648	P650	P852	P854	P856	P858	**P860**
Production	**1989**	**1991**	**1993**	**1995**	**1997**	**1999**	**2001**
Generation	**1.00**	**0.80**	**0.50**	**0.35**	**0.25**	**0.18**	**0.13 mm**
Gate Length	**1.00**	**0.80**	**0.50**	**0.35**	**0.20**	**0.13**	**0.07 mm**
SRAM Cell	**220**	**111**	**44**	**21**	**10.6**	**5.6**	**2.09 mm^2**
Supply	**5.0**	**5.0**	**3.3**	**2.5**	**1.8**	**1.5**	**1.3 volts**
# Metal	**2**	**3**	**4**	**4**	**5**	**6**	**6 (Copper)**

New generation every 2 years -
One reason why Intel is in leadership position

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130 Nanometer Technology Features

- 70nm (0.07mm) transistor gate & 1.5nm gate oxide
  - World's smallest, fastest transistor gate - the foundation of fast microprocessors
  - Thinnest gate oxide in the industry
  - Both allow for greater transistor density and faster performance
- Technology operates at 1.3 volts or less
  - 20% lower voltage than today's state-of-the-art technologies; excellent power performance for mobile computers

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130nm Technology Features

- Copper interconnects with low-k dielectrics
  - 130nm process means smaller die size, more die per wafer, lower cost
  - High aspect ratio (thickness/width) ensures a strong electric signal
  - Fluorine-doped SiO_2 low-k dielectric (for interconnects) -- good insulation between metal layers keeps electric signals isolated
  - Copper + high aspect ratio + low-k dielectric = lower interconnect resistance and lower interconnect capacitance, resulting in up to 40% reduction in interconnect delay
- High-yielding 18 Mbit SRAMs with a 2.45μm^2 memory cell
  - 2.09μm^2 memory cell under development for next year
  - Smallest SRAM cell size published to date

The combination of these features results in smaller, cheaper, and higher performing processors

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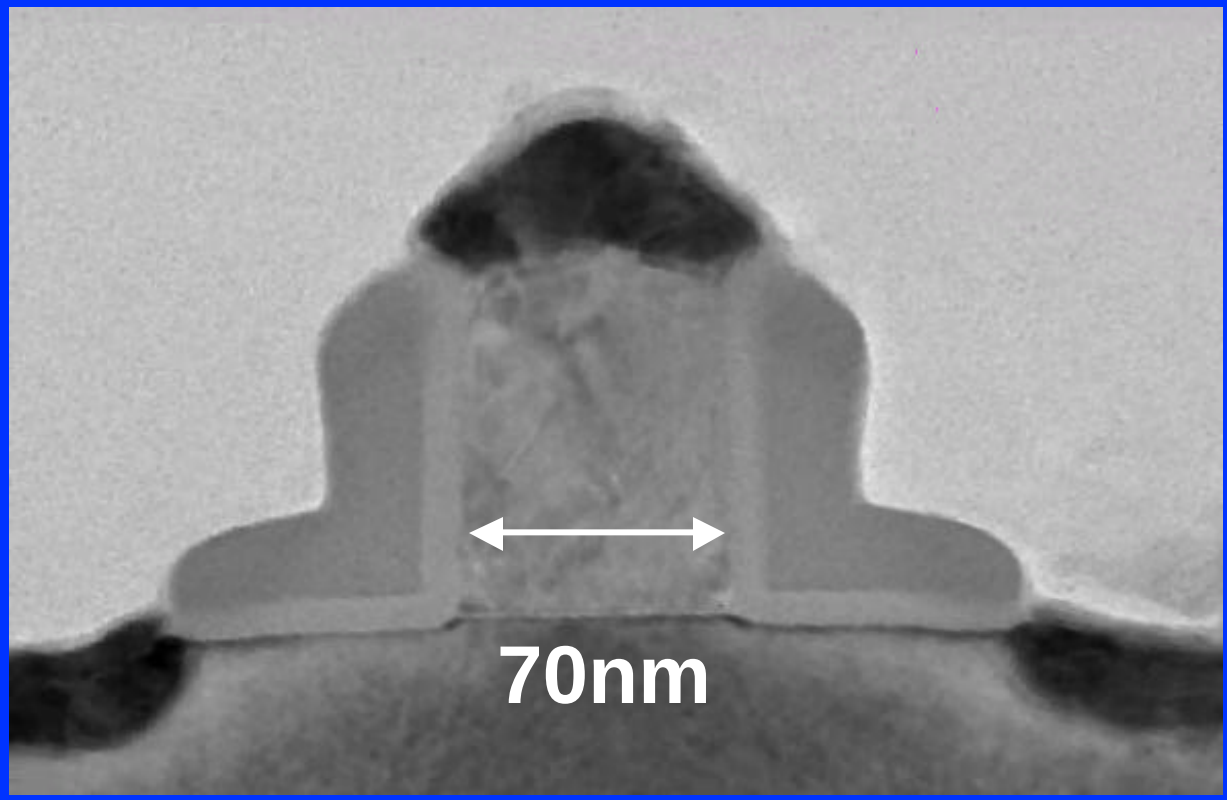
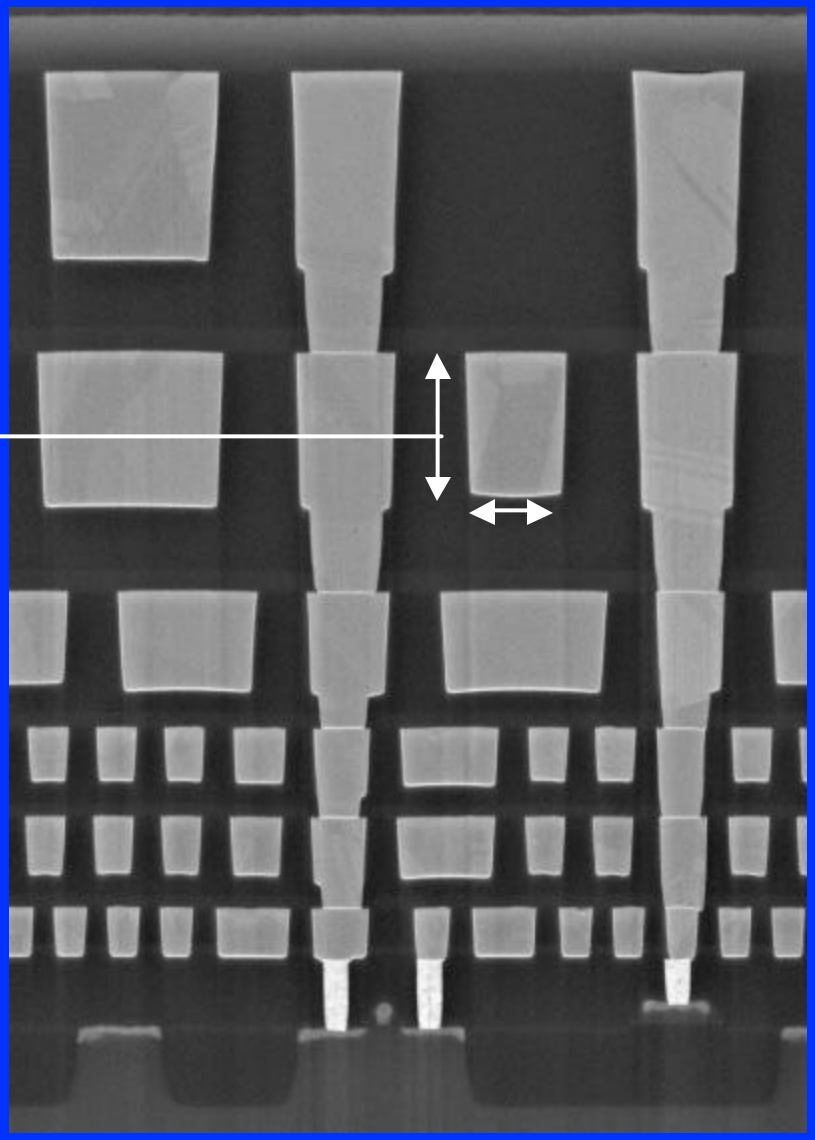
130nm Technology Features



70 nm L_{GATE} NMOS Transistor

Aspect Ratio
(T/W) = 1.6/1



Metal 6

Metal 5

Metal 4

Metal 3

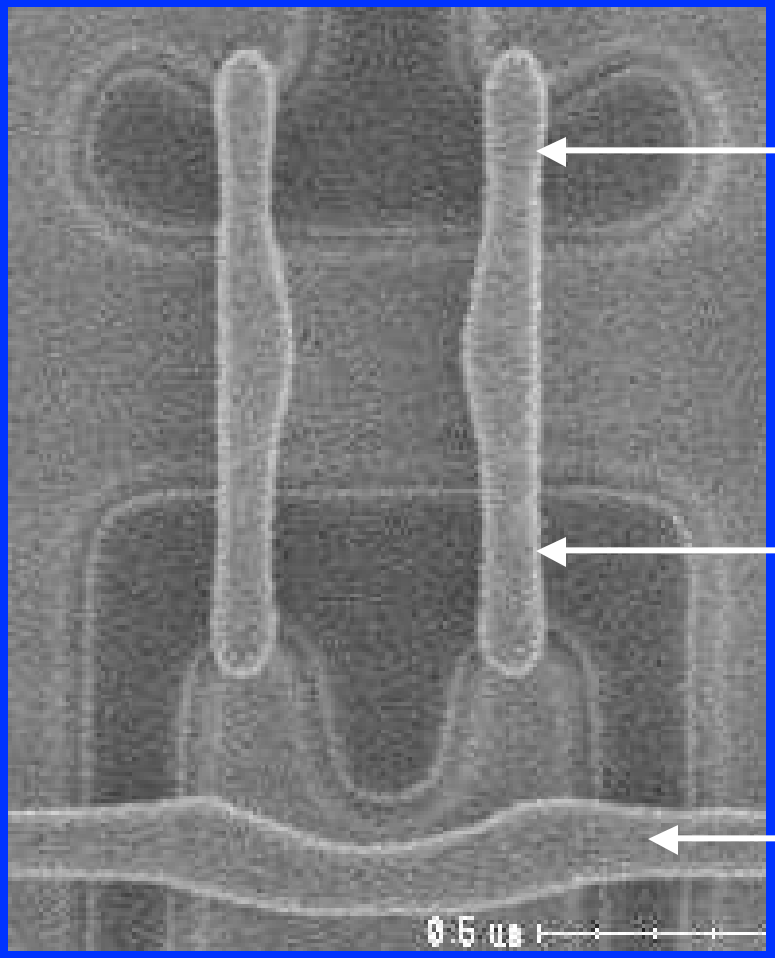
Metal 2

Metal 1

Transistors

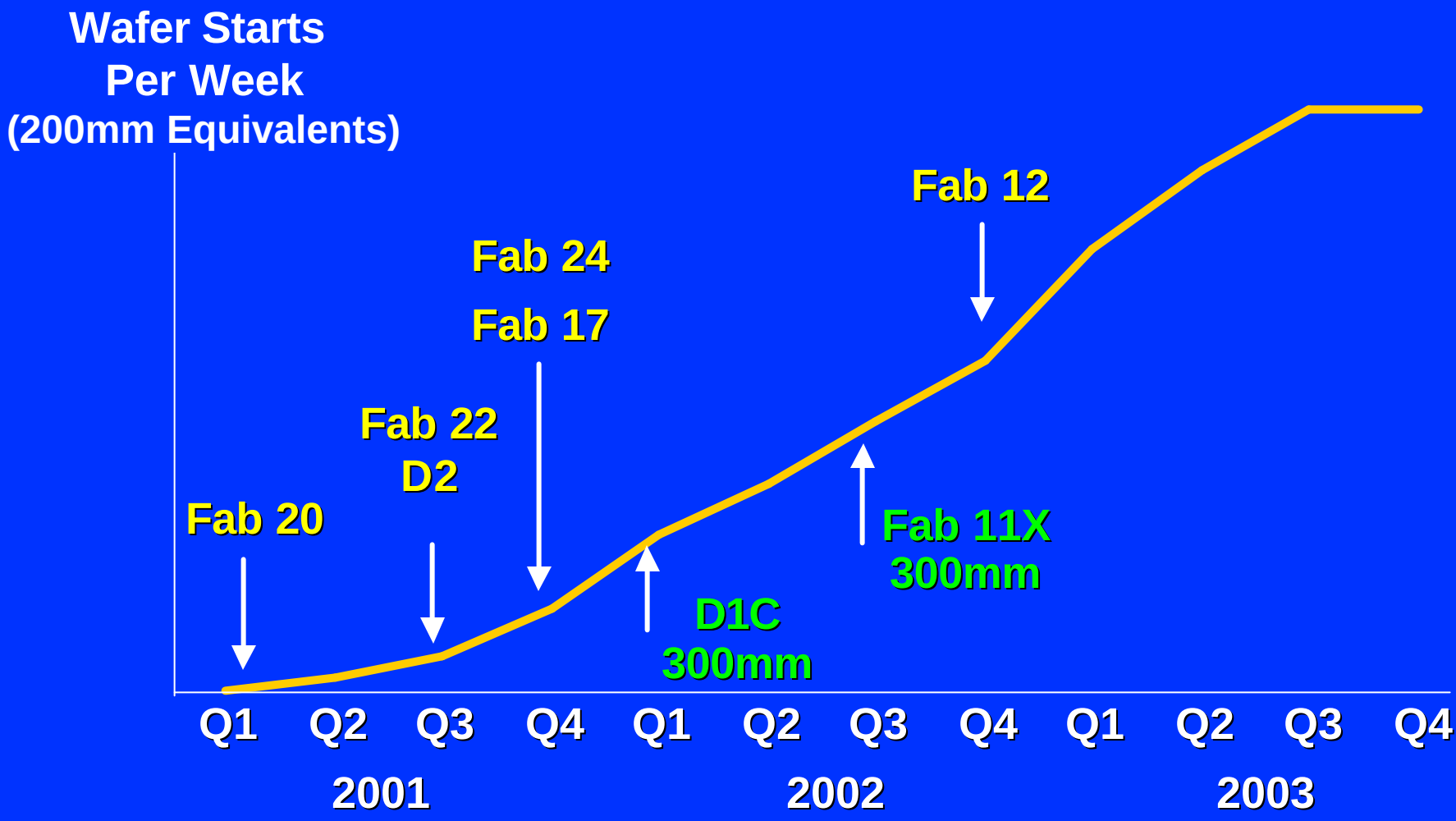
6 Layers of Damascene Copper

Damascene Copper Interconnects



2.09 μm² 6-Transistor SRAM Memory Cell

130nm Process Ramp in 8 Factories



Intel's Technology Edge

- Fastest transistors in the industry
- Copper and low-k interconnects
- Voltage scaling for low power
- Dense SRAM cell
- Functioning SRAMs, microprocessors
- Earliest 130nm production, 200/300mm
- > 100M transistor, multi-GHz products

Intel's logic technology continues to lead the industry

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Q & A

- For information on Intel's silicon technology, please visit the new Silicon Showcase at www.intel.com/research/silicon
- More 130nm technology details will be available at the IEEE International Electron Devices Meeting (IEDM) in San Francisco on December 12